Neuro-Space Mapping Technique for Nonlinear Device Modeling and Large Signal Simulation

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Abstract — **A new Neuro-Space Mapping (Neuro-SM) approach is presented enabling the space mapping (SM) concept to be applied to nonlinear device modeling and large signal circuit simulation. Suppose that an existing device model (namely, the coarse model) cannot match the actual device behavior (namely, the fine model). Using the proposed technique, the voltage and current signals between the coarse and the fine device models are mapped by a neural network. This mapping automatically modifies the behavior of the coarse model such that the mapped model accurately matches the actual device behavior. New training methods for such mapping neural networks are proposed. Examples of SiGe HBT and GaAs MESFET modeling and use of the models in harmonic balance simulation demonstrate that Neuro-SM is a systematic method to allow us to exceed the present capabilities of the existing device models.**

I. Introduction

Artificial Neural Networks (ANN) [1]-[3] and Space Mapping (SM) [4] are two recent developments in the microwave CAD area to address the growing challenges in modeling, simulation and optimization. Neural network computation is fast and it can be trained from data, allowing model development even when component formulas are unavailable [1]. Space mapping exploits mathematical link between fast yet approximate (coarse) models and accurate yet expensive (fine) models to achieve circuit design with the speed of coarse models and the accuracy of fine models [4]. Recently space mapping neuromodeling technique, combining neural networks with space mapping [5] was developed using neural networks to map the coarse model to fine model. The technique presently can be applied to passive modeling or small-signal device modeling, achieving fast and accurate models for such as bends, high temperature superconductor filters and embedded passives in multilayer printed circuits [5].

This paper expands the concept of space mapping neuromodeling to cover a new direction, i.e., large-signal dynamic nonlinear device modeling. Nonlinear device modeling is an important area of CAD, and many device models have been developed [6,7]. Due to rapid technology development in semiconductor industry, new devices constantly evolve. Models that were developed to fit previous devices may not fit new devices well. There is an ongoing need for new models. The challenges for CAD researchers are not only to develop more models, but also to innovate new CAD methods, so the task of developing models becomes more efficient and systematic. The latter aspect is the subject of this paper.

This paper presents a neuro-space mapping (Neuro-SM) technique, using a novel formulation of space mapping, to automatically modify the behavior of existing device models such that after modification the model accurately match new device data. This is made possible by a proposed neural network mapping to modify the voltage and current signals in the model. Examples of SiGe HBT and GaAs MESFET modeling and harmonic balance (HB) simulation demonstrate that the proposed Neuro-SM is a systematic method allowing us to exceed the present capabilities of existing device models.

II. Proposed Neuro-SM for Nonlinear Device Modeling

Coarse Model and Fine Model: Suppose that the existing/available models give only rough approximation of our device, and cannot accurately match the actual device data. Let the existing nonlinear device model be called the coarse model. The fine model in our case is only a fictitious model implied by actual device data from measurement or detailed/expensive device simulator.

Coarse Signal and Fine Signal: We use a 2-port device notation for our explanation. Let the terminal currents and voltage signals of the coarse device model be defined as $\boldsymbol{v}_c = [v_{c1}, v_{c2}]^T$ and $\boldsymbol{i}_c = [i_{c1}, i_{c2}]^T$, respectively. Let the terminal currents and voltages of the fine model be defined as $\boldsymbol{v}_f = [v_{f1}, v_{f2}]^T$, and $\boldsymbol{i}_f = [i_{f1}, i_{f2}]^T$, respectively. $\boldsymbol{v}_c$ and $\boldsymbol{i}_c$ are called coarse signals and $\boldsymbol{v}_f$ and $\boldsymbol{i}_f$ are called fine signals.

Neuro-SM: Fig. 1 shows the proposed Neuro-SM nonlinear 2-port network structure. The voltage signals for the overall model, i.e., v_{f1} and v_{f2} are not sent to the coarse model directly. Instead they are mapped (modified) into

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the voltages in the coarse model such that the modified coarse model response (say, i_c) will match the fine signal. Since the precise equation for this mapping is unknown, and the mapping in general can be nonlinear, a neural network becomes a logical choice as the realization of the mapping function. The input neurons for the neural network receives fine voltage signals v_{f1}, v_{f2}. The output neurons provides the mapped voltage signals for the coarse model, i.e., $v_c = f_{ANN}(v_f, w)$, where f_{ANN} represents the neural network and w is a vector containing all internal weights of the neural network. This neural network is then implemented as the functions in the voltage controlled voltage sources in our model shown in Fig. 1. We use current controlled current sources to pass i_c to i_f, in order to make the Neuro-SM model consistent with Kirchhoff's Laws as seen from the external terminals of the overall Neuro-SM model, which includes the coarse nonlinear model, all the controlled sources, and the neural network.

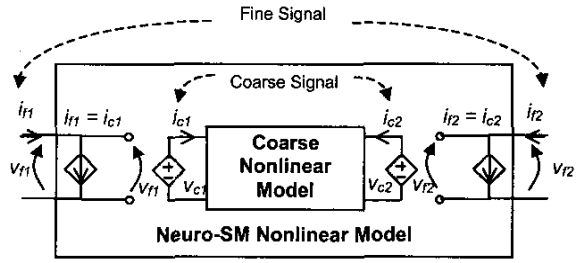


Fig 1. General 2-port Neuro-SM nonlinear model.

Cases of Mapping: For the Neuro-SM model to perform accurately, the neural network should be trained. However, available transistor data may not be directly in the form of instantaneous voltages (coarse and fine) for the input-output neurons as required by regular neural network training algorithms. Here we establish the connections of the proposed mapping with typical types of transistor data, such as DC, bias-dependent S-parameters and large-signal harmonic data, in order to formulate a new neural network training approach.

The proposed Neuro-SM model is a full large-signal nonlinear model. The mapping for DC voltages $V_{c,DC}$ and $V_{f,DC}$ is directly achieved by the neural network as:

$$V_{c,DC} = f_{ANN}(V_{f,DC}, w). \tag{1}$$

The small signal S-parameters are mapped via the mapping relationship of the Y matrices between the coarse model Y_c and fine model Y_f, as

$$Y_f = Y_c \cdot \left(\left. \frac{\partial f_{ANN}^T(v_f, w)}{\partial v_f} \right|_{v_f = V_{f,Bias}} \right)^T. \tag{2}$$

where the derivative of f_{ANN} is obtained at bias point $V_{f,Bias}$ using the adjoint neural network in Fig. 2. As for large-signal case, the mapping of harmonic signals between the coarse model $V_c(k\omega)$ and fine model $V_f(l\omega)$ is:

$$V_c(k\omega) = \frac{1}{N_T} \sum_{n=0}^{N_T-1} f_{ANN}\left(\sum_{l=0}^{N_H} V_f(l\omega) \cdot W_N^{-(l\omega)(nT)}, w \right) \cdot W_N^{(k\omega)(nT)}$$
$$k = 0, 1, \ldots, N_H. \tag{3}$$

where ω is fundamental frequency, N_H is number of harmonics, T is time interval and N_T is the number of time points. W_N is defined as $e^{-j2\pi}$.

Training of Neuro-SM Model: The overall training has two phases, initialization and formal training. In the initialization phase, we first initialize the neural network by a preliminary training to learn unit mapping, i.e., $v_c = v_f$. Training data can be obtained by assigning $[v_{c1}, v_{c2}]$ in a grid form across the entire operation range of the device. This initialization phase guarantees that the overall Neuro-SM model is equal to the coarse model, before actual device data is used in the formal training of the neural network. In the formal training phase, the neural network internal weights w are adjusted such that the Neuro-SM model matches device data better than the coarse model does. In this way, for a given device model, the proposed Neuro-SM model automatically exceeds or at least equals the performance of the given coarse model.

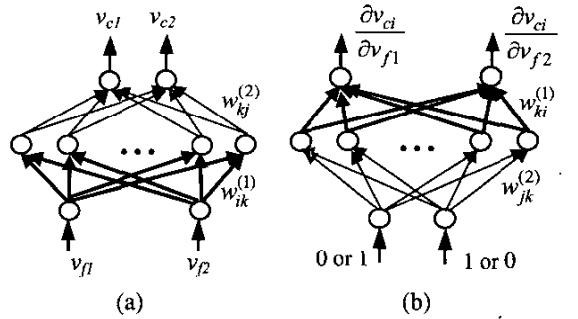


Fig. 2. (a) Original neural network $v_c = f_{ANN}(v_f, w)$ and (b) adjoint neural network in Neuro-SM. (a) is used for DC and large-signal mapping and (b) is used for small-signal mapping. Vector w contains all weights $w^{(1)}{}_{ik}$ and $w^{(2)}{}_{kj}$, where i, k, j are indices of neurons in the input, hidden and output layers in (a). The adjoint neural network structure corresponds to a flip of the original neural network between inputs and outputs. The output of adjoint neural network is $\partial v_{ci} / \partial v_f$ where i=1 or 2 if the adjoint inputs are [1, 0] or [0, 1], respectively.

The overall training error can be the total difference between all available device data (such as DC and bias-dependent S-parameters) and the Neuro-SM model. The derivative of the training error versus neural network

weights needed by neural network training algorithms is obtained by differentiating the mapping relationships of (1)-(3) with the derivative part in the coarse model done through circuit sensitivity techniques and the derivative part for f_{ANN} done through adjoint neural network sensitivity [8].

Use of Neuro-SM Model: After training, the Neuro-SM model can be used by user or circuit simulator. The neural network internal weights w are fixed. The voltage/current relationship of the model required by user or circuit simulator is that between v_f and i_f, which is obtained from Neuro-SM model through the mapping of coarse model signals as defined in Figure 1.

III. Examples

A. Neuro-SM Nonlinear Model for SiGe HBT Device

This example shows how Neuro-SM works in a simple DC case of a SiGe HBT device modeling, with data from measurement [9]. The coarse model used is a standard Curtice model [10]. The internal parameters of the coarse model are first optimized. However, the coarse model at its best provides only approximation of the device and lacks the complicated details seen in the device data in Fig. 3. We applied the proposed Neuro-SM technique. The base current and collector voltage are mapped onto the coarse model, and these mapped signals then excite the coarse model, resulting in an improved value of collector current. Simulation result comparison is shown in Fig 3. The neural network used 55 hidden neurons. In general, fewer (more) hidden neurons are needed if the coarse model is good (poor). This example demonstrates that using Neuro-SM technique, a basic Curtice model originally developed for GaAs FETs can now be automatically extended beyond its original limitation to match the highly irregular nonlinear behavior in the SiGe HBT example.

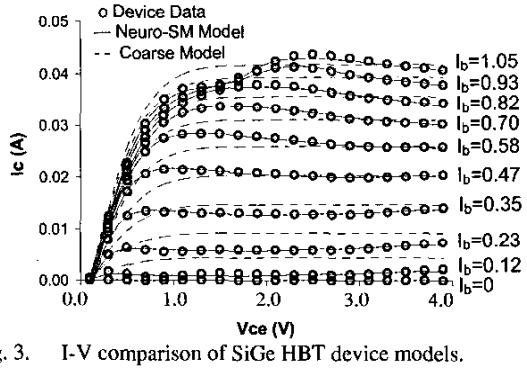


Fig. 3. I-V comparison of SiGe HBT device models.

B. Neuro-SM Nonlinear Model for GaAs FET Device

This example illustrates a full large signal Neuro-SM model trained with both DC and bias dependent S-parameter data. The fine device data is generated from an ADS internal GaAs FET model [11, 12]. The Curtice cubic model [10] is used as coarse model. There are clear differences between the coarse model and the fine device data, which cannot disappear even after the parameters in the coarse model are optimized as much as possible. We will use our proposed Neuro-SM to automatically adjust the coarse model to match the fine device data. Fig. 4 shows the structure of this Neuro-SM nonlinear model.

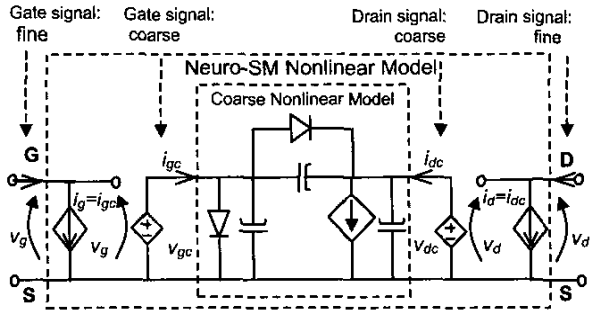


Fig. 4. Structure of Neuro-SM GaAs FET Nonlinear Model.

Training was done using both DC and S-parameter data at 150 bias points in the range (Vg: -1 to 0V, Vd: 0 to 5V, and frequency: 1 to 20 GHz). The number of hidden neurons used was 10. After training, we compare the Neuro-SM nonlinear model with the coarse model and the original ADS data. The result is plotted in Fig.5, showing clear improvements using Neuro-SM over the coarse model. For comparison purpose, we also trained a pure neural network model (device entirely modeled by dynamic neural network (DNN) [13] without use of any equivalent circuit). Table I gives the comparison of accuracy and extrapolation capability between the models. Two sets of data are used with 10% and 20% derivation beyond bias and frequency range for extrapolation test. The proposed Neuro-SM model outperforms the pure neural network model when the model is used outside its training range.

TABLE I
TEST ERROR (%) COMPARISON

Model Type	Within training range		Extrapolation beyond training range (10%/20%)
	Before training	After training	
Pure Neural Model	133.34	1.38	36.25/43.81
Coarse Model	10.57	10.57	10.36/10.44
Neuro-SM Model	10.57	1.46	1.87/2.03

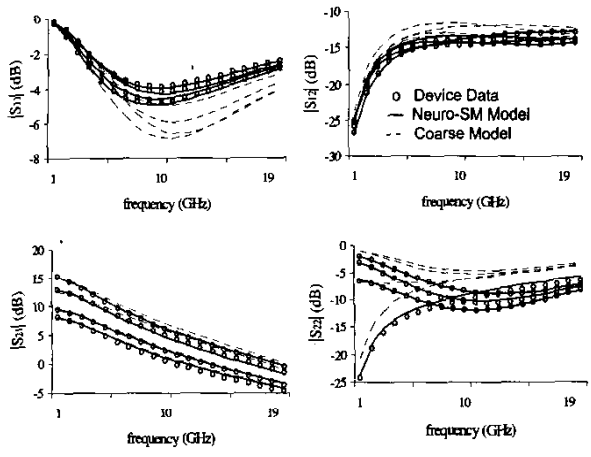
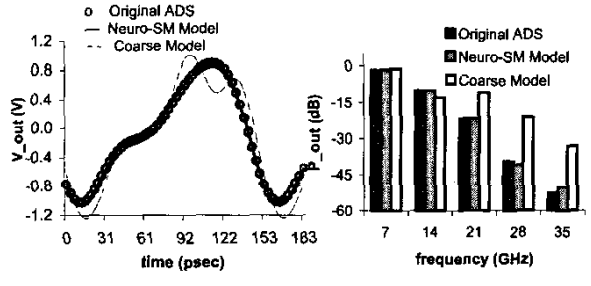


Fig. 5. S-parameter comparison of GaAs FET model at 4 different biases.

C. Use of Neuro-SM Model in Amplifier Design

In this example, we use the trained Neuro-SM GaAs FET nonlinear model of section III.*B* in a three-stage power amplifier simulation and optimization. The power amplifier is from [8]. We performed large-signal harmonic balance simulation of the amplifier, and the result matches well with the original ADS solutions, shown in Fig. 6. This verifies the validity of the large-signal behavior of the proposed Neuro-SM device model. To further demonstrate the use of the model, we also performed yield optimization and Monte-Carlo analysis with 1000 statistical outcomes of the three-stage amplifier using the Neuro-SM models with 53 geometrical parameters of all the passive components in the amplifier as variables. The yield evaluated after optimization using coarse model and the proposed model is 26% and 70%, respectively. The original ADS optimal yield is 73%. This further confirms that the Neuro-SM model can be used to help statistical analysis and optimization.



(a) (b)

Fig. 6. Time domain response (a), and frequency domain harmonic balance response (b) of the three stage amplifier using original ADS solution, Neuro-SM model and coarse model.

IV. Conclusion

By modifying the voltage/current signals fed to the model using Neuro-SM, we can automatically improve an existing model of coarse accuracy into a new model of fine accuracy. For the first time, computer-based automatic modification of existing large-signal device models now becomes achievable, avoiding otherwise trial and error based manual modification of models. This work is also aimed at efficient and automatic updating of nonlinear device model libraries as new semiconductor technologies continue to evolve.

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